Multilayer Ceramic Capacitors

[Large Size Capacitors]

LCC Series

◆ Features

- ❑ Optimized internal designs offers the highest voltage rating (up to 8KVdc)
- ❑ Capacitance range from 100pF to 18uF and sizes from 2520 to 3640
- ❑ Available with proprietary surface coating for arc prevention
- ❑ Available with flexible termination (Super Term) to minimize the effects of mechanical stress
- ❑ RoHS compliant

◆ Applications

- ❑ Voltage Multipliers
- ❑ Power Supplies
- ❑ DC-DC Converters
- ❑ Surge protection
- ❑ Industrial control circuits
- ❑ Isolation
- ❑ Ballast
- ❑ Snubber
- ❑ Custom applications

◆ Summary of Specifications

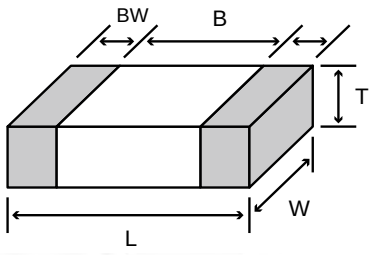
Operation Temperature	-55 ℃ ~ +125 ℃	
Rated Voltage	50Vdc ~ 8KVdc	
Temperature Coefficient	NP0 : ≤ ± 30ppm/ ℃ , -55 ~ +125 ℃ (EIA Class I)	
	X7R : ≤ ± 15% , -55 ~ +125 ℃ (EIA Class Ⅱ)	
Capacitance Range	NP0 : 68pF ~ 220nF , X7R : 1000pF ~ 18uF	
Dissipation Factor	NP0 : Q≧1000 , X7R : 2.5% max.	
Insulation Resistance	10GΩ or 500/CΩ, whichever is smaller (C in Farad)	
Aging	NP0 : 0% , X7R : 2.5 % per decade of time	
Dielectric Strength	V ≤ 500V	: 200% Rated Voltage
	500V ≤ V < 1000V	: 150% Rated Voltage
	V ≥1000V	: 120% Rated Voltage

◆ How To Order

C	2520	X	103	K	102	T	N	S	X	Y
Product Code	**Chip Size**	**Dielectric**	**Capacitance Unit : pF**	**Tolerance**	**Rated Voltage**	**Packaging**	**Termination**	**Testing Requirement**	**Special Requirement**	**Suffix Code**
C: MLCC (Multilayer Ceramic Capacitor)	Ex.: 2520 3530 3640	Ex.: N : NP0 X : X7R	Ex.: 100 : $10x10^0$ 471 : $47x10^1$ 102 : $10x10^2$	Ex.: J : +/- 5% K : +/-10% M : +/-20%	Ex.: 050:50Vdc 251:250Vdc 102:1000Vdc 202:2000Vdc	Ex.: T : T&R W : Waffle B : Bulk	Ex: N: Ni Barrier / Sn Plate	Ex.: S: Standard Electrical	Ex.: O: Arc Prevention Coating X: Polymer Termination (Super Term) Z: Coating & Polymer Termination	Y

Dimension

Unit : mm [inches]



SIZE	L	W	T (max)	B (min)	BW (min)
2520	6.35±0.50 [.25±.020]	5.00±0.50 [.20±.020]	3.2 [.126]	4.0 [.157]	0.3 [.012]
3330	8.4±0.50 [0.33±0.2]	7.6 ±0.50 [0.30±0.2]	4.0 [.157]	4.0 [.157]	0.3 [.012]
3530	8.90±0.50 [.35±.020]	7.60±0.50 [.30±.020]	5.0 [.200]	5.5 [.217]	0.3 [.012]
3640	9.20±0.50 [.36±.020]	10.20±0.50 [.40±.020]	5.0 [.200]	6.0 [.236]	0.3 [.012]

Capacitance Range

Size	Dielectric	Capacitance (pF) maximum									
		50V	100V	250V	500V	1KV	2KV	3KV	4KV	5KV	8KV
2520	NP0	823	683	563	473	103	392	222	102	471	101
	X7R	685	685	395	474	334	563	473	822	822	152
3330	NP0	224	184	104	683	333	823	392	292	821	251
	X7R	126	126	825	105	824	124	823	183	183	332
3530	NP0	224	184	104	823	473	103	472	332	102	251
	X7R	126	126	825	105	824	124	823	183	183	332
3640	NP0	224	184	104	823	473	123	562	392	122	561
	X7R	186	186	106	125	105	184	104	273	273	392

- ***All values are capacitance EIA codes.***
- ***Other dimensions, capacitance values and voltages rating are available. Please contact Holy Stone.***

Soldering And Handling Precautions:

Large ceramic capacitors are more prone to thermal and mechanical cracks. To minimize mechanical cracks, capacitors have to be handled carefully in the original waffle pack container, carrier tape or other suitable container. Care must be taken that these capacitors do not come into contact with each other which can cause chip outs, cracks or other mechanical damage.

The recommended method for soldering large chips is reflow soldering. Wave soldering and manual soldering with Iron is not recommended. Ceramic capacitors must be preheated with less than 2°C/second rate to about 50°C below the reflow temperature. Any sudden increase or decrease in temperature more than the recommended rate, during soldering, may cause internal thermal cracks.

Options:

- Holy Stone offers polymer termination (Super Term) for very large chips to minimize mechanical cracks due to board flexing.
- To minimize the potential for surface arcing in higher voltage applications, IHHEC offers the option of a proprietary surface coating.