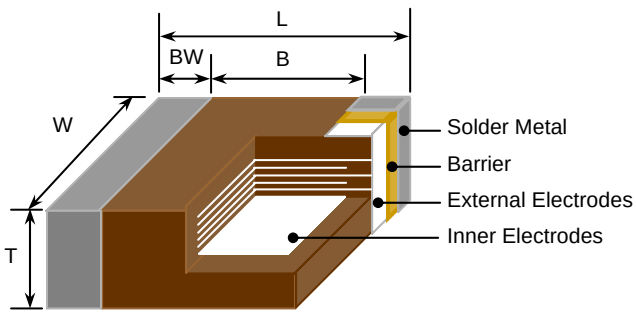
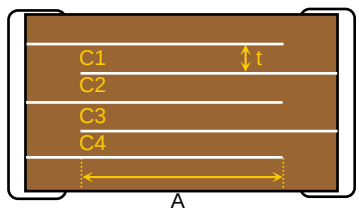
The Multilayer Ceramic Chip Capacitors supplied in bulk, cassette or taped & reel package are ideally suitable for thick-film Hybrid circuits and automatic surface mounting on printed circuit boards.

MLCC's are mainly used in electronic circuits for by-pass, filtering and smoothing circuit.

◆ Construction and Physical Dimension



Cross Section



Dimensions(mm) [inches]

EIA style	L	W	Tmax.	BWmin	Bmin.
0201	0.60±0.03 [.024±.002]	0.30±0.03 [.011±.002]	0.33 [.013]	0.10 [.004]	0.20 [.008]
0402	1.00±0.05 [.039±.002]	0.50±0.05 [.020±.002]	0.55 [.022]	0.15 [.006]	0.30 [.012]
0603	1.60±0.10 [.063±.004]	0.80±0.10 [.031±.004]	0.90 [.035]	0.15 [.006]	0.40 [.016]
0805	2.00±0.20 [.079±.008]	1.25±0.25 [.049±.008]	1.45 [.057]	0.20 [.008]	0.70 [.028]
1206	3.20±0.30 [.126±.012]	1.60±0.20 [.063±.008]	1.80 [.071]	0.30 [.012]	1.50 [.059]
1210	3.20±0.30 [.126±.012]	2.50±0.20 [.098±.008]	2.60 [.102]	0.30 [.012]	1.60 [.063]
1808	4.60±0.30 [.181±.012]	2.00±0.20 [.079±.008]	2.20 [.087]	0.30 [.012]	2.50 [.098]
1812	4.60±0.30 [.181±.012]	3.20±0.30 [.126±.012]	3.00 [.118]	0.30 [.012]	2.50 [.098]
1825	4.60±0.30 [.181±.012]	6.35±0.40 [.250±.016]	2.60 [.102]	0.30 [.012]	2.50 [.098]
2208	5.70±0.40 [.220±.016]	2.00±0.20 [.197±.008]	2.20 [.087]	0.30 [.012]	3.50 [.137]
2211	5.70±0.40 [.220±.016]	2.80±0.40 [.110±.016]	3.00 [.118]	0.30 [.012]	3.50 [.137]
2220	5.70±0.40 [.220±.016]	5.00±0.40 [.197±.016]	3.00 [.118]	0.30 [.012]	3.50 [.137]
2225	5.70±0.40 [.220±.016]	6.35±0.40 [.250±.016]	3.00 [.118]	0.30 [.012]	3.50 [.137]

$$C = \varepsilon_0 \cdot \varepsilon \frac{A \cdot N}{t}$$

C : Capacitance
ε_0 : Dielectric constant in the air
ε : Proportional dielectric constant
A : Overlap Area
t : Dielectric Thickness
N : Layers

◆ Nominal Capacitance and Tolerance

1. Standard Combination of Nominal Capacitance and Tolerance

Class	EIA Symbol	Tolerance	Nominal Capacitor
I	NPO	J (±5%),K (±10%)	E-12 ,E-24 Series
Π	X7R	K(±10%), M(±20%)	E-3,E-6 Series
	X7E	K(±10%), M(±20%)	E-3,E-6 Series
	X5R	K(±10%), M(±20%)	E-3,E-6 Series
	Y5U	M(±20%),Z(+80/-20 %)	E-3 Series
	Y5V	M(±20%),Z(+80/-20 %)	E-3 Series
	Z5U	M(±20%),Z(+80/-20 %)	E-3 Series

2. E Series (Standard Number)

E-Series	Application Capacitance											
E-3	1.0				2.2				4.7			
E-6	1.0		1.5		2.2		3.3		4.7		6.8	
E12	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
E24	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
	1.1	1.3	1.6	2.0	2.4	3.0	3.6	4.3	5.1	6.2	7.5	9.1

◆EIA Designations

For Class IDielectrics

Coefficient of capacitance (ppm/ ℃)		Multiplier applicable to column		Tolerance of temp. coeff.(ppm/ ℃)	
0.0	C	-1.0	0	30	G
1.0	M	-10	1	60	H
1.5	P	-100	2	120	J
2.2	R	-1000	3	250	K
3.3	S	-10000	4	500	L
4.7	T	+1	5	1000	M
7.5	U	+10	6	2500	N
		+100	7		
		+1000	8		
		+10000	9		

Ex.: C0G Negative 0±30ppm/ ℃
U2J Negative 750±120ppm/ ℃

For Class Π Dielectrics

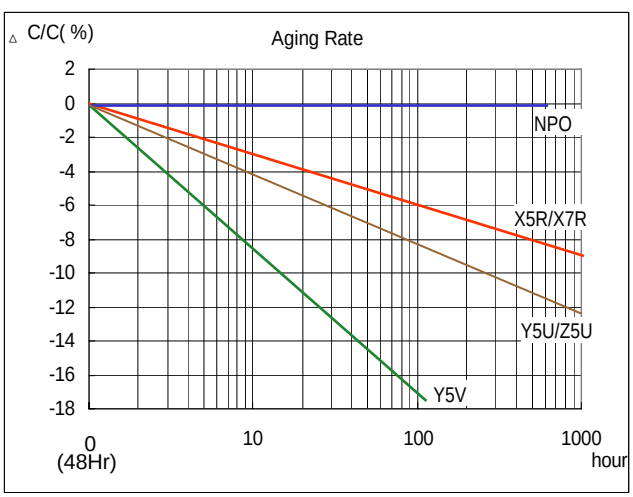
Low Temp. Symbol		High Temp. Symbol		Max. %△C Symbol	
-55℃	X	+45℃	3	±1.0%	A
-30℃	Y	+65℃	4	±1.2%	B
+10℃	Z	+85℃	5	±2.2%	C
		+105℃	6	±3.3%	D
		+125℃	7	±4.7%	E
		+150 ℃	8	±7.5%	F
		+200 ℃	9	±10.0%	P
				±15.0%	R
				±22.0%	S
				+22% /-33%	T
				+22% /-56%	U
				+22% /-82%	V

Ex.: X7R -55 ~ +125 ℃ ±15%
Y5V -30 ~ +85 ℃ +22%/-82%

◆ Operation Temperature Range

Class	EIA Symbol	Dielectric Code	Temperature Range(℃)	Capacitance Change	Reference Temperature
I	NPO	N	-55℃ ~ +125 ℃	0±30 ppm/℃	20℃
Π	X7R	X	-55℃ ~ +125℃	±15%	20℃
	X7E	C	-55℃ ~ +125℃	±4.7%	25℃
	X5R	B	-55℃ ~ +85℃	±15%	20℃
	Y5V	Y	-30℃ ~ +85℃	+22/-82 %	20℃
	Y5U	E	-30℃ ~ +85℃	+22/-56 %	25℃
	Z5U	Z	+10℃ ~ +85℃	+22/-56 %	25℃

◆ Dielectric Material – Aging Rate



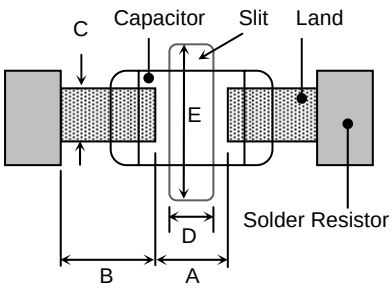
Aging Rate
NPO: 0
X7R/X5R : 2 ~ 4 % /decade
Y5U/Z5U : 4~6% / decate
Y5V : 6~10 % /decade

After performing De-Aging at 150±5 ℃ for 30 minutes and placement room temperature for 48 hours.

◆ Recommended Board Pattern

Improper circuit layout and pad/land size may cause excessive or not enough solder amount on the PC board. Not enough solder may create weak joint, and excessive solder may increase the potential of mechanical or thermal cracks on the ceramic capacitor. Therefore we recommend the land size to be as shown in the following table:

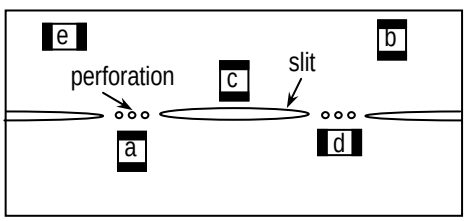
1. Size and recommend land dimensions for reflow soldering



EIA Code	Chip (mm)		Land (mm)				
	L	W	A	B	C	D	E
0201	0.60	0.30	0.2~0.3	0.2~0.4	0.2~0.4	--	--
0402	1.00	0.50	0.3~0.5	0.3~0.5	0.4~0.6	--	--
0603	1.60	0.80	0.4~0.6	0.6~0.7	0.6~0.8	--	--
0805	2.00	1.25	0.7~0.9	0.6~0.8	0.8~1.1	--	--
1206	3.20	1.60	2.2~2.4	0.8~0.9	1.0~1.4	1.0~2.0	3.2~3.7
1210	3.20	2.50	2.2~2.4	1.0~1.2	1.8~2.3	1.0~2.0	4.1~4.6
1808	4.60	2.00	2.8~3.4	1.8~2.0	1.5~1.8	1.0~2.8	3.6~4.1
1812	4.60	3.20	2.8~3.4	1.8~2.0	2.3~3.0	1.0~2.8	4.8~5.3
1825	4.60	6.35	2.8~3.4	1.8~2.0	5.1~5.8	1.0~4.0	7.1~8.3
2208	5.70	2.00	4.0~4.6	2.0~2.2	1.5~1.8	1.0~4.0	3.6~4.1
2211	5.70	2.80	4.0~4.6	2.0~2.2	2.0~2.6	1.0~4.0	4.4~4.9
2220	5.70	5.00	4.0~4.6	2.0~2.2	3.5~4.8	1.0~4.0	6.6~7.1
2225	5.70	6.35	4.0~4.6	2.0~2.2	5.1~5.8	1.0~4.0	7.1~8.3

2. Mechanical strength varies according to location of chip capacitors on the P.C. board.

Design layout of components on the PC board must be such a way to minimize the stress imposed on the components, upon flexure of the boards in depanelization or other processes.

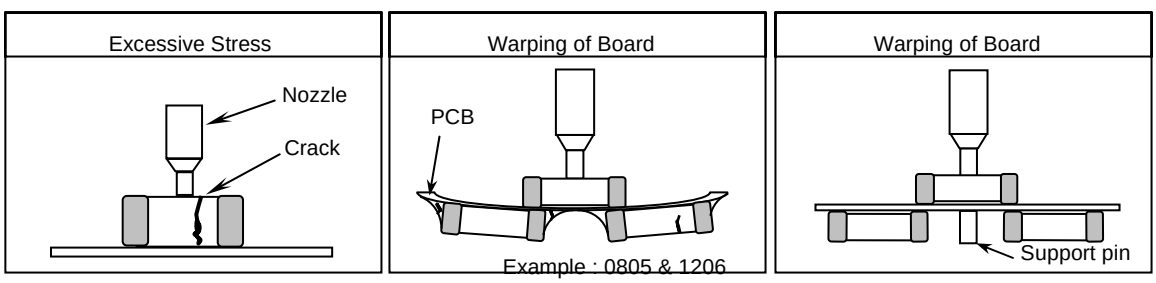


Component layout close to the edge of the board or the "depanelization line" is not recommended.
Susceptibility to stress is in the order of: a>b>c and d>e

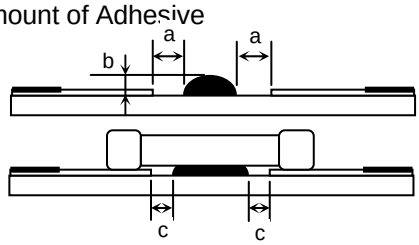
◆ Mounting

1. Sometimes crack is caused by the impact load due to suction nozzle in pick and place operation.

In pick and place operation, if the low dead point is too low, excessive stress is applied to component. This may cause cracks in the ceramic capacitor, therefore it is required to move low dead point of a suction nozzle to the higher level to minimize the board warp age and stress on the components. Nozzle pressure is typically adjusted to 1N to 3N (static load) during the pick and place operation.



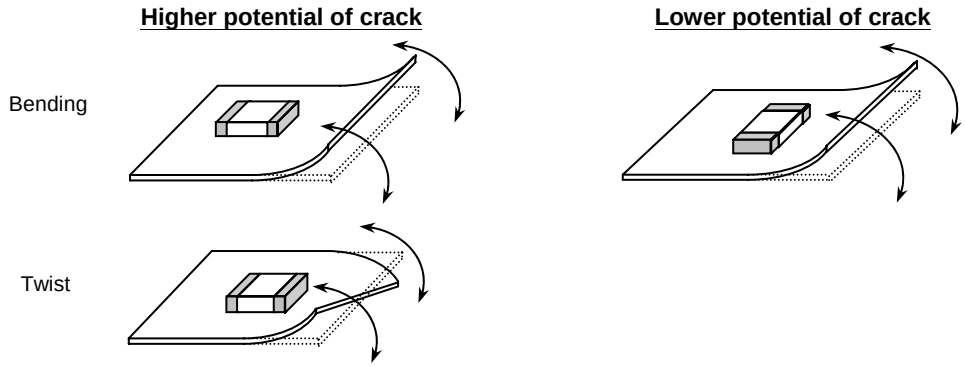
2. Amount of Adhesive



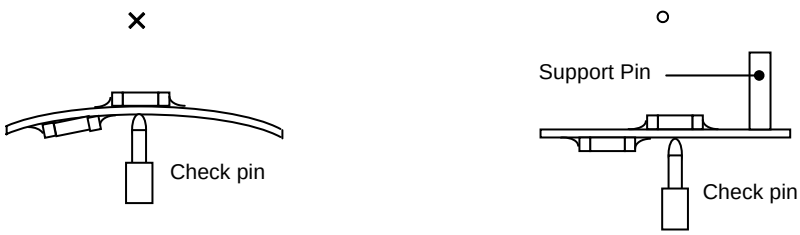
a	0.2mm min.
b	70 ~ 100 μm
c	Do not touch the solder land

◆ Handling after chip mounted

1. Proper handling is recommended, since excessive bending and twist of the board, depends on the orientation of the chip on the board, may induce mechanical stress and cause internal crack in the capacitor.

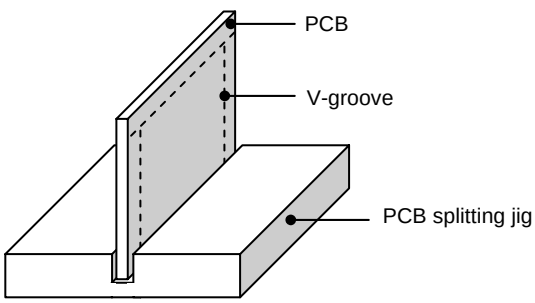


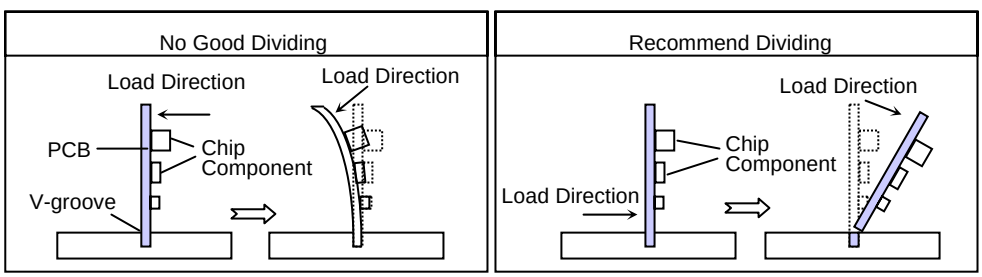
2. There is a potential of crack if board is warped due to excessive load by check pin



3. Examples of PCB dividing/breaking jigs:

The outline of PCB breaking jig is shown below. It is recommended when dividing or breaking PCB that they are held near the jig where no bending will occur, this way there will be no compressive stress applied to the components on the PCB. Do not hold the PCB at a position which is far away from the jig, tensile stress to the components may cause them to crack.



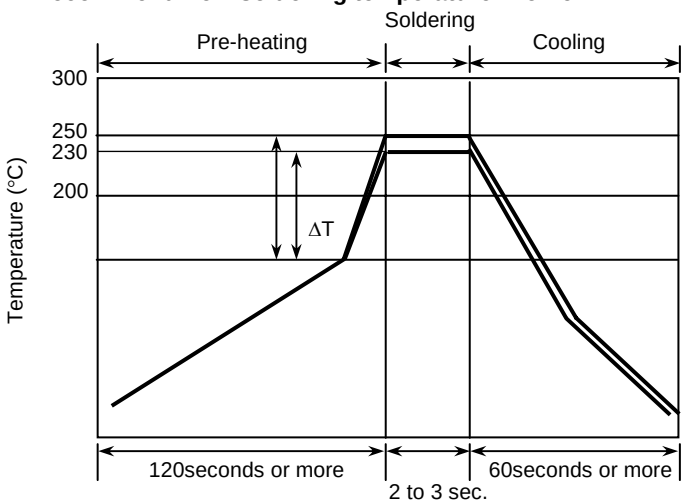


◆Soldering

1. Wave Soldering

Most of components are wave soldered with solder at 230 to 250°C. Adequate care must be taken to prevent the potential of thermal cracks on the ceramic capacitors. Refer to the soldering methods below for optimum soldering benefits.

Recommend flow soldering temperature Profile



Soldering Method	Change in Temp.(℃)
1206 and Under	ΔT ≤100~130℃max.

To optimize the result of soldering, proper preheating is essential:

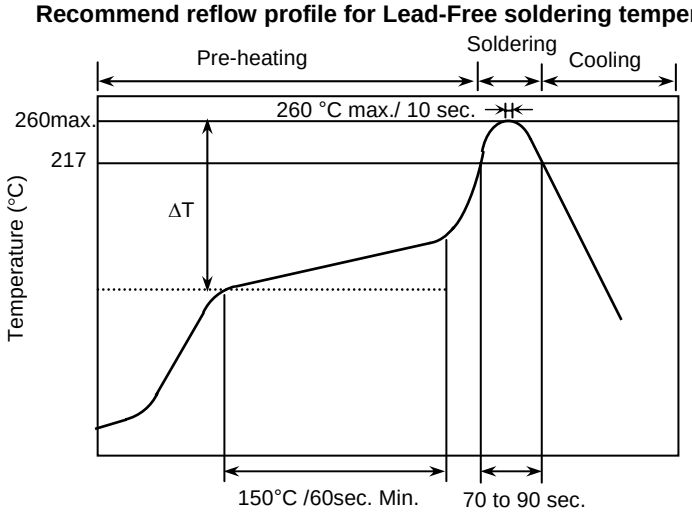
1) Preheat temperature is too low
   a. Flux flows to easily
   b. Possibility of thermal cracks
2) Preheat temperature is too high
   a. Flux deteriorates even when oxide film is removed
   b. Causes warping of circuit board
   c. Loss of reliability of chip and other components

Cooling Condition:
Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) between the solvent and the chips must be less than 100°C.

2. Reflow Soldering

Preheat and gradual increase in temperature to the reflow temperature is recommended to decrease the potential of thermal crack on the components. The recommended heating rate depends on the size of component, however it should not exceed 3°C/Sec.

Recommend reflow profile for Lead-Free soldering temperature Profile (MIL-STD-202G #210F)

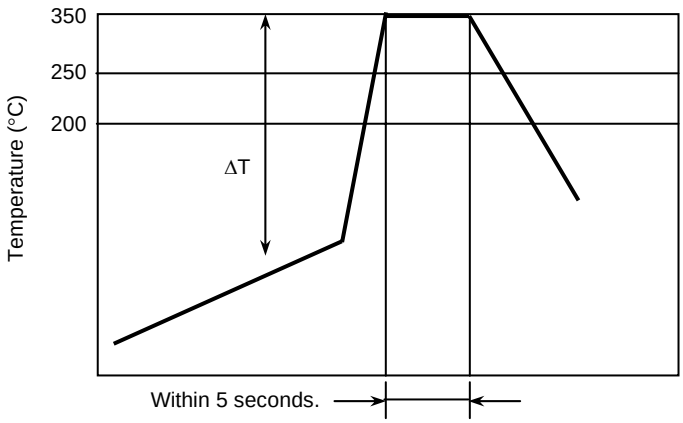


Soldering Method	Change in Temp.(℃)
1206 and Under	ΔT ≤190℃
1210 and Over	ΔT ≤130℃

※ The cycles of soldering : Twice (Max.)

3. Hand Soldering

Sudden temperature change in components, results in a temperature gradient recommended in the following table, and therefore may cause internal thermal cracks in the components. In general a hand soldering method is not recommended unless proper preheating and handling practices have been taken. Care must also be taken not to touch the ceramic body of the capacitor with the tip of solder Iron.



Soldering Method	Change in Temp.(℃)
1206 and Under	ΔT ≤150℃
1210 and Over	ΔT ≤130℃

How to Solder Repair by Solder Iron

1) Selection of the soldering iron tip

The required temperature of solder iron for any type of repair depends on the type of the tip, the substrate material, and the solder land size.

2) recommended solder iron condition

a.) Preheat the substrate to (60°C to 120°C) on a hot plate. Note that due to the heat loss, the actual setting of the hot plate may have to be higher. (For example 100°C to 150°C)

b.) Soldering iron power shall not exceed 30 W.

c.) Soldering iron tip diameter shall not exceed 3mm.

d.) Temperature of iron tip shall not exceed 350°C of Value,and the process should be finished within 5 seconds. **(refer to MIL-STD-202G)**

e.) Do not touch the ceramic body with the tip of solder iron. Direct contact of the soldering iron tip to ceramic body may cause thermal cracks.

f.) After soldering operation, let the products cool down gradually in the room temperature.

◆Storage

Store the capacitors where the temperature and relative humidity don't exceed 40°C and 70%RH. We recommend that the capacitors be used within 6 months from the date of manufacturing. Store the products in the original package and do not open the outer wrapped, polyethylene bag, till just before usage. If it is open, seal it as soon as possible or keep it in a desiccant with a desiccation agent.